MICRO-428: Metrology

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MICRO-428: Metrology

Week Twelve: Electrical Metrology

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Reference Books

📖 B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill., 2017

Week 11 Summary

11.1 Noise reduction: filtering; averaging techniques – effect on signal and noise:

$Var\{N_{avg}\} = \frac{1}{n}\sigma^2$ and $SNR_{avg,identical\ sign.} = n\ SNR$ (replicate measurements, signal $s(t)$ uncorrelated to noise, and noise $z(t)$ uncorrelated; also valid when there are different (additive) independent noise sources)

11.2 Electric Signals, Analog-to-Digital Conversion: Sampling and Holding (S/H), Quantizing and Encoding (Q/E)

Parameters: resolution, Differential non-linearity (DNL), Integral non-linearity (INL), Quantization noise ($\sigma^2_{noise} = {\Delta^2}/{12}$), Signal-to-quantization-noise ratio ($SQNR = 20log_{10}(2^Q) \approx 6.02 \cdot Q + 1.76$)

ADC architectures: Integrating, Successive-Approximation, (Charge-redistribution,) Flash (Direct Conversion), Pipelined

The lecture starts with a small recap of the main elements of the previous week.

Week 11 Summary

11.3 Timing – Time-to-Digital Conversion: Non-idealities, DNL, INL, optical tests (single-shot precision, code density test)

TDC architectures: Counter – Register, Delay Chain, Vernier Lines, Ring Oscillator

Application Examples: Time-resolved imaging (ToF, FLIM, PET, Raman, …)

Technique: Time-correlated single-photon counting (TCSPC)

Outline

Outline

It’s now time to look at one very important component of modern electronics circuits, the PLL. We’ll then study how it can be used to measure very weak signals buried in noise by means of a lock-in amplifier. The lecture will then be wrapped up by a quick look at other tools for electrical metrology.

12.1.1 PLL: Phase-locked Loop

- Phase-locked Loop (PLL) is an Electronic Module (control circuit) that locks the phase of the output to the input (which also implies keeping the input and output frequencies the same) -> coincident rise (fall) edges
- «The PLL helps keep parts of our world orderly.» (*Henri de Bellescize, 1932)*
- «If we turn on an analogue television set, a PLL will keep heads at the top on the screen and feet at the bottom. In color television another PLL makes sure that green remains green and red remains red even if the politicians claim that the reverse is true. » (attributed to *Henri de Bellescize*)
- Why do I need it if I already have an input signal?

  Examples of uses: Frequency Multiplications (with the base accuracy of the reference), Clock Skew and/or Jitter Reduction (to counteract inter/intra-chip propagation errors)

Q

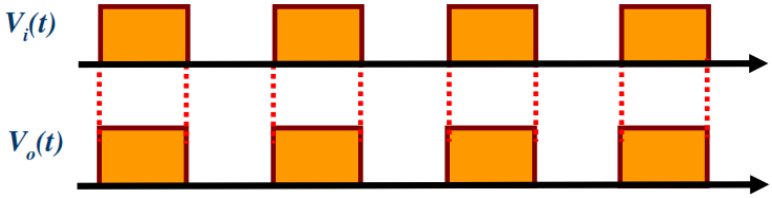
B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

This is a brief description of what a PLL is and what it does. The last bullet contains some application examples. Note that the difference between **skew** (basically a fixed offset → concept of accuracy) and **jitter** (a random fluctuation in time → concept of precision) should be clear by now, as well as their implications.

You can think of repetitive signals in the time domain, such as a clock, and how they move in time from one instance to the next.

12.1.1 PLL Basics

- Example of locked phase:



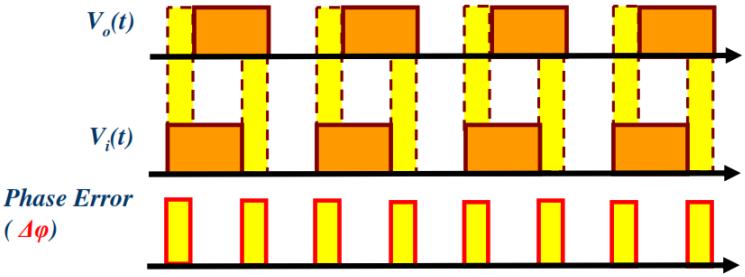
B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

The input signal might be for example generated off-chip, and the output one directly on-chip. Here they have the same frequency, but this needs not be. The input signal can usually not be propagated as such within the chip or other electronic component, nor can it be generated on-chip directly with the required precision.

The important thing is that the output tracks the input.

12.1.1 PLL Basics

- Example of unlocked phase:

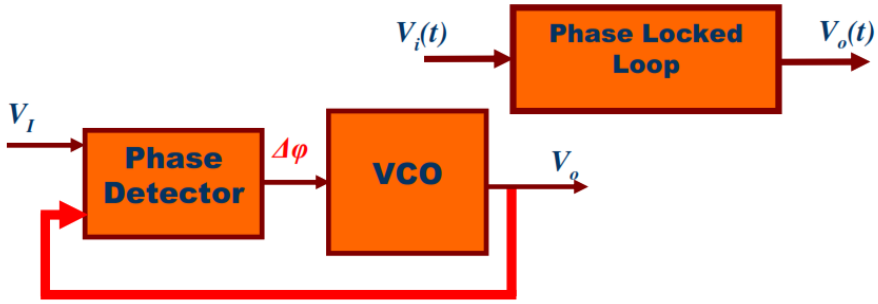


B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

Here we illustrate a typical example of what happens when there is a phase error – which usually needs to be corrected – between the two signals.

12.1.1 PLL Basics – Phase detector + VCO

- PLL is a feedback system that detects the phase error $\Delta\varphi$ and then adjusts the phase of the output.



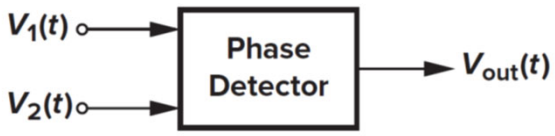
- Phase Detector (PD) detects $\Delta\varphi$ between the output and the input through a feedback system.
- Voltage-Controlled Oscillator (VCO) adjusts the phase difference.

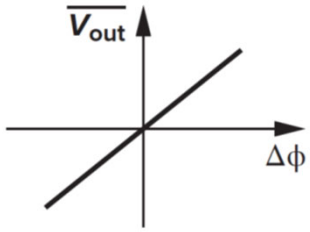
📖 B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

Illustrated here are the main components of a simple PLL.

12.1.1 PLL – Phase Detector

- A phase detector is a circuit whose average output is linearly proportional to the phase difference, $\Delta\varphi$, between its two inputs ($V_1(t)$ and $V_2(t)$).
- In the ideal case, the relationship between V_{out} and $\Delta\varphi$ is linear, crossing the origin for $\Delta\varphi = 0$.





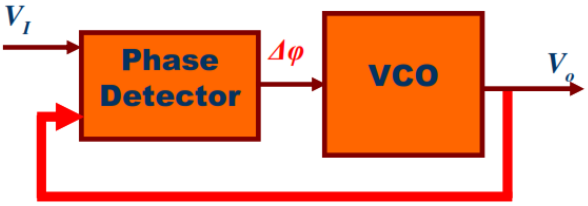
B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

Let's first focus on the phase detector and its characteristics.

12.1.1 PLL – Phase Detector (XOR Gate)

- A familiar example of phase detector is the exclusive OR (XOR) gate.

Q



$$\Delta\varphi = \begin{cases} 1 & V_I \neq V_o \\ 0 & V_I = V_o \end{cases}$$

V_0	V_1	$\Delta\phi$
0	0	0
0	1	1
1	0	1
1	1	0

- As the phase difference between the input varies, so does the width of the output pulses, thereby providing a DC level proportional to $\Delta\varphi$.

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

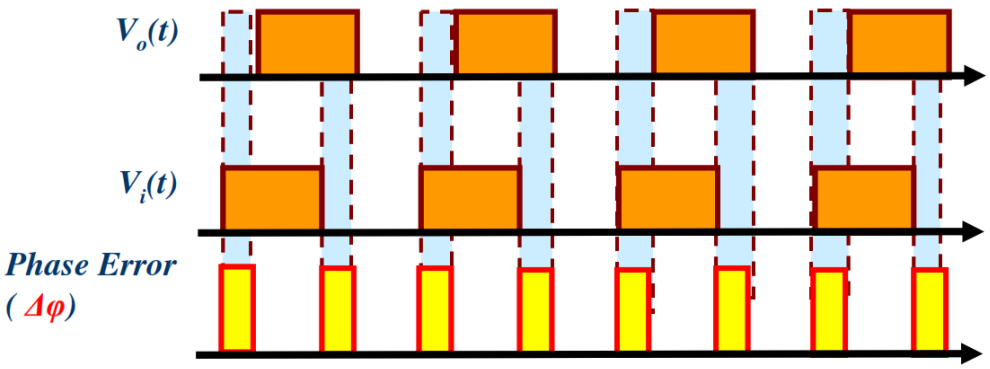
A simple example of a phase detector is a XOR gate.

→ Do you remember its truth table?

It outputs true whenever the inputs differ, which is exactly the kind of behaviour which we want.

12.1.1 PLL – Phase Detector (XOR Gate)

XOR example



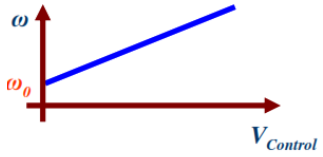
- While the XOR circuit produces error pulses on both rising and falling edges, other types of Phase Detectors may respond only to positive or negative transitions.
- The operation of phase detectors is similar to that of differential amplifiers in that both sense the difference between the two inputs, generating a proportional output.

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

This is an example of the output of a XOR gate. Note that it is active whenever there is a difference between the two signals.

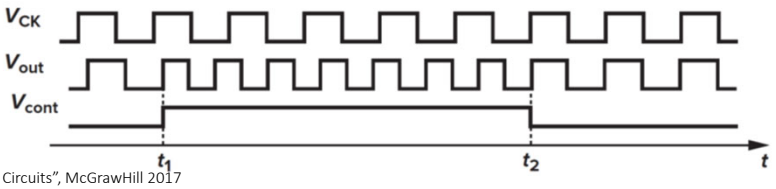
12.1.1 PLL – Voltage-Controlled Oscillator (VCO)

- VCO is a circuit model that oscillates at a controlled frequency ω.
- The Oscillating Frequency is controlled using voltage $V_{control}$.



$$\omega = \omega_o + K_{VCO} V_{Control}$$

- Note: if we have a single control input ($V_{control}$), we must vary the frequency to vary the phase!



B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

We now turn our attention to a VCO, the second main component. Note that the VCO does not directly control the phase, which is the reason why we state that "we must vary the frequency to vary the phase" (if we have a single control input).

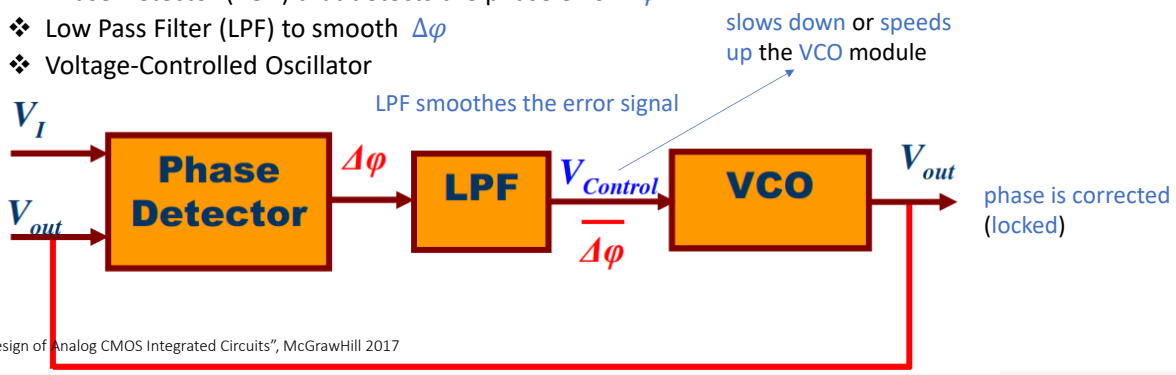
An example is provided in the bottom picture, which shows how the signals can get again in a lock condition.

12.1.1 Simple PLL

- $V_{control}$ must be in the steady state («remain quiet») for the VCO to operate properly. However, the Phase Detector output, i.e. the phase error $\Delta\varphi$, consists of a dc component (desirable) and high-frequency components (undesirable) -> filtering of Phase Detector output needed.

  -> Simple PLL consists of three basic functional blocks:

  - ❖ Phase Detector (XOR) that detects the phase error $\Delta\varphi$
  - ❖ Low Pass Filter (LPF) to smooth $\Delta\varphi$
  - ❖ Voltage-Controlled Oscillator



B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

In practical systems, a low pass filter is needed to smoothen the error signal.

Q: can you identify the DC and high-frequency components in the output of the XOR gate, e.g. at slide 14?

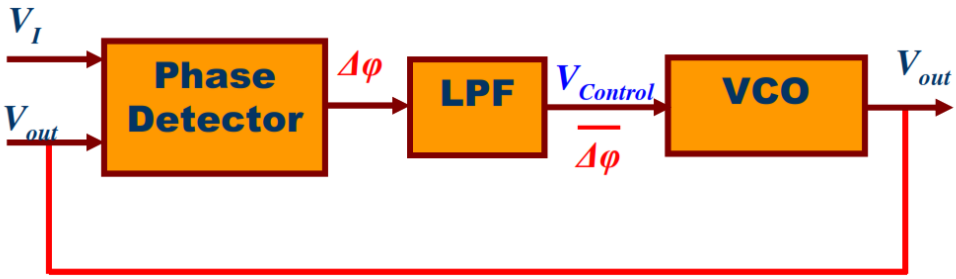
12.1.1 PLL - Locked Condition

- Locked Condition:

$$\phi_{out}(t) - \phi_{in}(t) = \text{constant} \rightarrow \frac{d}{dt}(\phi_{out} - \phi_{in}) = 0$$

- This implies that

$$\omega_{in} = \omega_{out}$$



- An important and unique consequence of phase locking is that the input and output frequencies of the PLL are exactly equal.

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

Note the phase locking condition and its consequence, in terms of $\omega_{in} = \omega_{out}$.

NB: the constant is not necessarily always equal to 0, although that's a typical condition.

12.1.1 PLL - Locked Condition, Small Transients

- For simplicity, let's assume:

Locked conditions $V_{in} = V_A \cos(\omega_1 t)$,
$V_{out} = V_B \cos(\omega_1 t + \varphi_0)$
+ phase error (e.g. a phase step):
$\Delta\varphi = \phi_1 u(t - t_1) \rightarrow \phi_{in} = \omega_1 t + \phi_1 u(t - t_1)$

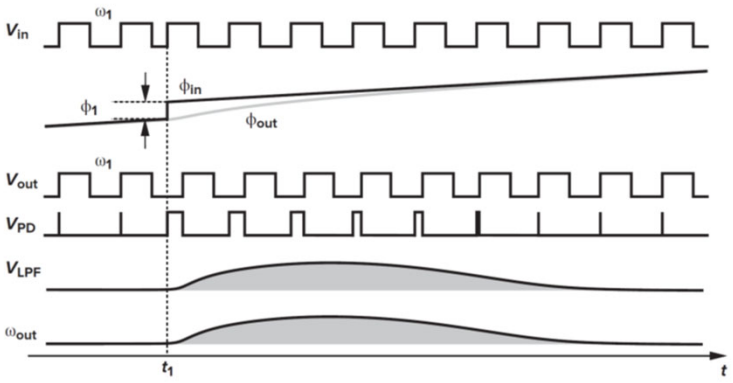
-> The Phase Detector creates $V_{control}$ and VCO will change:

$$\omega_{out} = \omega_1 + K_{VCO} V_{Control}$$

- When the loop settles, the output voltage becomes:

$$V_{out} = V_B \cos\big(\omega_1 t + \varphi_0 + \Delta\varphi(t)\big)$$

Response of a PLL to a phase step



$V_{Control}$ rises gradually, VCO frequency begins to change
Loop is not locked during the transient ($\Delta\varphi$ varies with time)
ω_{out} must eventually go back to ω_1
ϕ_{out} gradually catches up with ϕ_{in}
All the parameters assume their original values

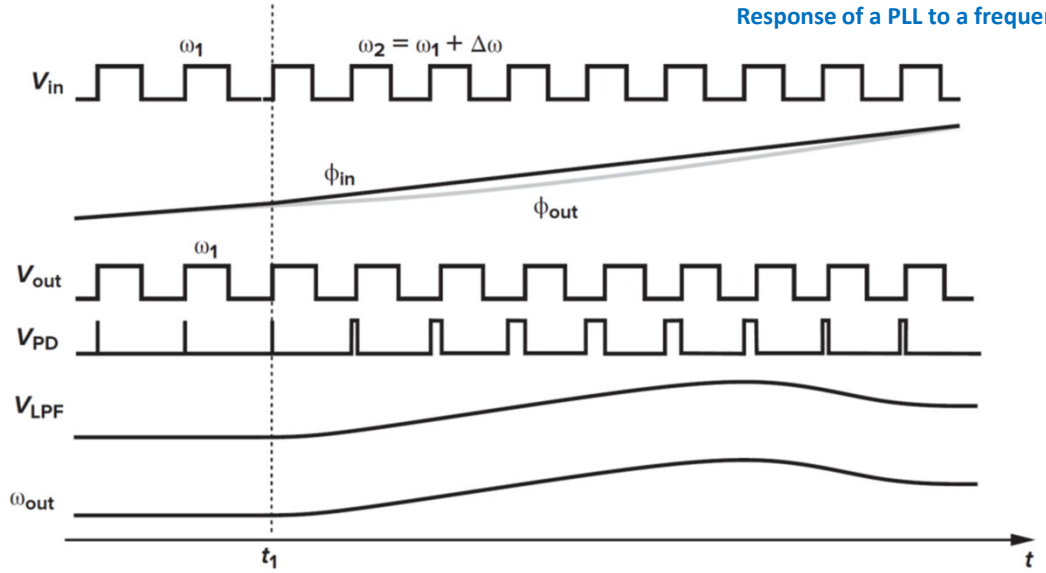
B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

Let's now look at how a PLL behaves in certain scenari, for example when the input signal undergoes **a phase step at constant frequency** ω_1, as shown in the top line of the image. At the end of the process the output voltage does track again the input one.

[Razavi par. 16.1 p. 657:] higher harmonics are neglected!

12.1.1 Dynamics of Simple PLL (transient behaviour)

Response of a PLL to a frequency step



B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

In this other example, the input voltage changes frequency ("frequency step"), e.g. accelerating (higher frequency, $\omega_2 > \omega_1$). In this case ω_{out} does eventually settle to the higher value, ω_2.

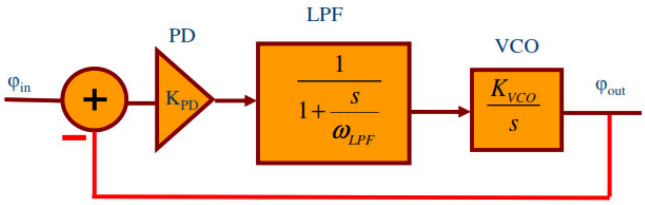
12.1.1 Dynamics of Simple PLL (transient behaviour)

S

- Exact transient (settling) behaviour in general: PLL is a feedback system

  -> Linear model:

  PD is a gain amplifier
  LPF is a first order filter (as an example)
  VCO is a unit step module



B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

In practice one would need to model the exact PLL dynamics to determine how fast the PLL settles, in particular during the start phase, or how fast it dampens possible transients. These aspects will not be studied in detail and are only left here for completeness (see the small "S" in the top right corner).

12.1.1 Dynamics of Simple PLL (transient behaviour)

- The (closed loop) transfer function of the system (which determines how the output phase tracks the input phase) will be:

$$H(s) = \frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + K_{PD}K_{VCO}\omega_{LPF}}$$

which we can rewrite as (ω_n = natural frequency, ζ = damping factor):

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

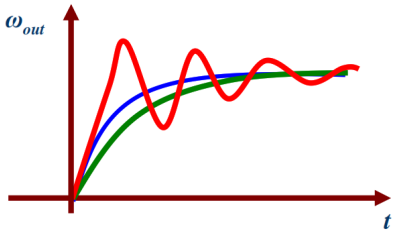
(2nd order transfer function, two poles)

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

12.1.1 Transient response of a PLL

- Unit (frequency) step response of a second order system:

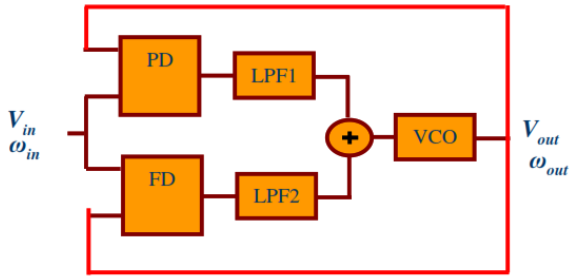
Overdamped
Critically damped
Underdamped



B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

12.1.1 PLL Lock Acquisition Problem

- Suppose that, when the PLL is turned on, the output frequency is far from the input frequency
- It is possible that the PLL would never lock
- Modern PLL uses Frequency Detector (FD) in addition to the Phase Detector (PD)



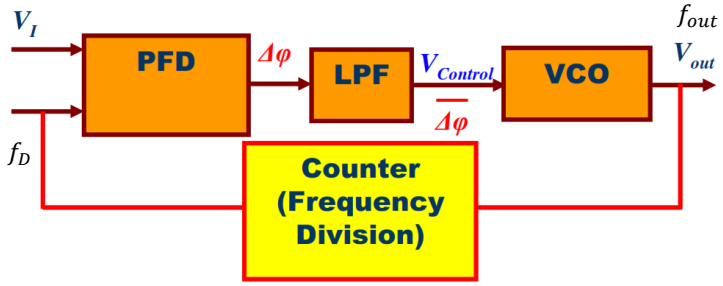
At the beginning, the FD drives ω_{out} toward ω_{in} while the PD output remains "quiet." When $|\omega_{out} - \omega_{in}|$ is sufficiently small, the phase-locked loop takes over, acquiring lock.

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

12.1.1 PLL Applications

1. Frequency Multiplications (PLL multiplies input frequency by M):

- The feedback loop has frequency division
- Frequency division is implemented using a counter (one output pulse every M input pulses)



$f_{out} = Mf_{in}$

$f_D = f_{out}/M$

https://www.youtube.com/watch?v=kOAUpw0W138 (16:00)

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

The PLL section will be concluded with the illustration of typical applications.

The first one – **frequency multiplication** – is of fundamental importance and allows to generate (much) higher precise frequencies, e.g. on-chip. The underlying working principle is not immediately obvious but nicely illustrated in the YouTube video (bottom right link).

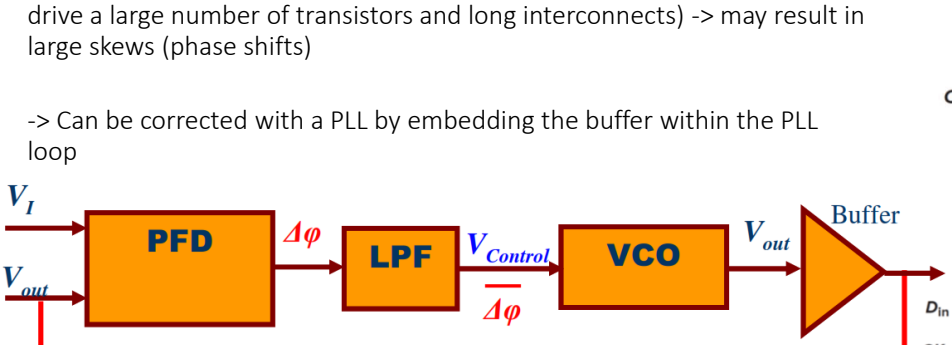
As an example, think of the case where we have a 1MHz input and a division by 10 → the VCO has to generate a 10MHz output – which will be divided into 1MHz at f_D – to lock. De facto we are multiplying the input frequency by 10x!

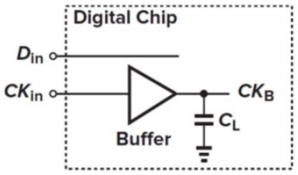
12.1.1 PLL Applications

2. Clock Skew Reduction

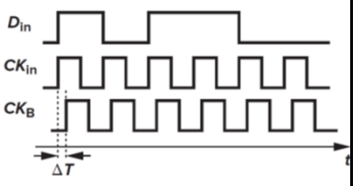
Buffers (buffer amplifiers) are routinely used to distribute the clock (to drive a large number of transistors and long interconnects) -> may result in large skews (phase shifts)

-> Can be corrected with a PLL by embedding the buffer within the PLL loop





D = data, CK = clock



B. Razavi, "Design of Analog CMOS Integrated Circuits", McGrawHill 2017

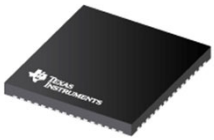
Another possible application is clock skew reduction, e.g. when distributing clock signals within a large chip. In this case buffers need to be used to amplify the clock signal at periodic intervals, but these do typically introduce delays, i.e. skews, as shown in the bottom right image.

12.1.1 PLL Applications

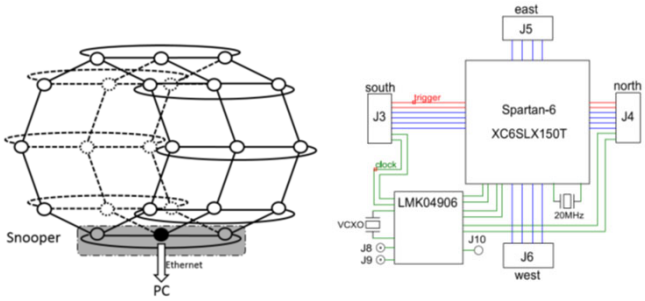
3. Jitter Reduction

PLL ASIC example: LMK04906 (Texas Instruments) Ultralow Noise Clock Jitter Cleaner and Multiplier With 6 Programmable Outputs

- Input clock: <500MHz
- Output clocks: 284kHz to 2.6GHz
- Internal VCO frequency: 2.6GHz
- Dual Loop PLL architecture
- 25-ps Step Analog Delay Control
- …



Texas Instruments, LMK04906 - https://www.ti.com/lit/ds/symlink/lmk04906.pdf



Example of use for clock jitter cleaning and phase offset compensation in a clock distribution network for Positron Emission Tomography (PET)

Front side: Tile of the first generation SPADnet sensor

Back side: FPGA board and Power distribution

C. Bruschini, C. Veerappan, et al., A Sensor Network Architecture for Digital SiPM-Based PET Systems, IEEE TRPMS 2, 2018

A final example is **jitter reduction** – specific chips like the one shown on the left, embedding one or more PLLs, can be used to "clean" the jitter of input signals and/or compensate their offset (skew) in programmable fine steps, for example to take into account different lengths of the traces on a PCB or of cables (different lengths = different delays).

Such chips can also handle multiple outputs (fan-out). This allows to generate multiple signals with similar clock characteristics. Tree-like configurations are also possible, thus multiplying the total number of outputs.

Right: example of a concrete application in search PET set-up, where information on the detected events was propagated in a ring-like structure from one element to the next, looking for coincidences. Given that the timing precision is of outmost importance, PLL-based elements like the chip on the left were embedded in each sensor node.

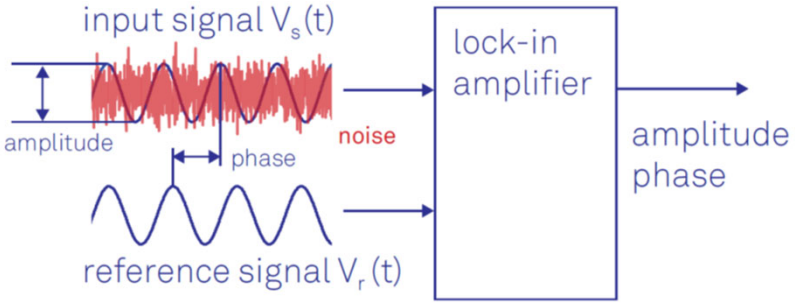
Outline

12.1.2 PLL Application Example: Lock-in Amplifier

*Also: noise is often spread over a much wider range of frequencies than the signal

- Amplifier which can extract a signal with a known carrier wave from an extremely noisy environment (signals up to 10^6 smaller, in amplitude, than noise = 120 dB!) -> concept of dynamic reserve.
- Trick: use knowledge about a signal's time dependence, or impose it*.

- Is basically a homodyne detector (i.e. single frequency) followed by a low-pass filter that is often adjustable in cut-off frequency and filter order.
- Traditional (analog): analog frequency mixers and RC filters for the demodulation,
- Digital: digital signal processing, for example, on an FPGA.



$V_r(t)$ (internal reference signal) is usually generated by a PLL locked to the external reference

EN Wikipedia *Lock-in amplifier; Zurich Instruments Lock-in white paper*

Signal extraction from a large noise background is indeed possible, and does often rely on some knowledge about the signal's time dependence – or on imposing it. *There is always a trick somewhere…*

In this example the signal $V_s(t)$ is buried in the red background noise. $V_r(t)$ – the internal reference signal of the lock-in amplifier – is usually generated by a PLL locked to the external reference.

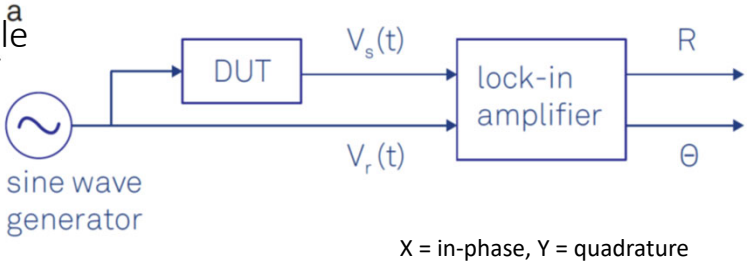
12.1.2 Lock-in Amplifier: Principle

A) Typical lock-in set-up: a sinusoidal signal drives the device under test (DUT) and serves as a reference signal. The lock-in outputs the amplitude and phase relative to the reference signal.

B) "Down-mixing": the input signal is multiplied by the reference signal and a 90◦ phase-shifted version of the reference signal (sine and cosine demodulation – dual-phase demodulation) ->.

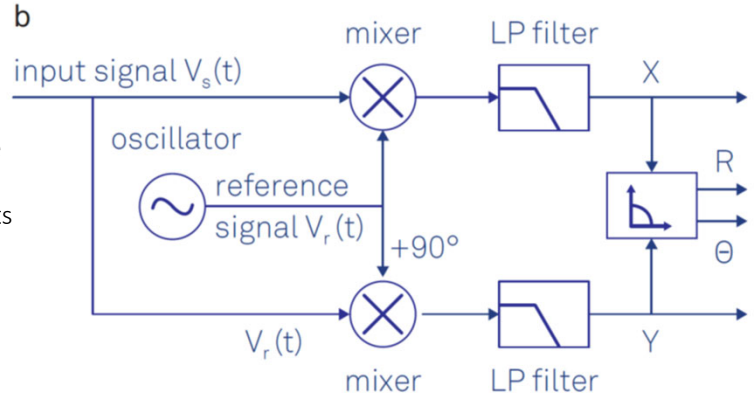
C) "Demodulation": the mixer outputs are low-pass filtered to reject the noise and the 2ω component, and finally converted into polar coordinates.

a



X = in-phase, Y = quadrature

b



EN Wikipedia *Lock-in amplifier; Zurich Instruments Lock-in white paper*

12.1.2 Lock-in Amplifier: Principle

$$V_s(t) = R \cdot \cos(2\pi f_s t + \phi_s), V_r(t) = \cos(2\pi f_r t)$$

Q Mixing: $V_s(t) \cdot V_r(t)$

-> Two components at $(f_s\text{-}f_r)$ and $(f_s\text{+}f_r)$.

- If f_r=f_s: $(f_s\text{-}f_r)$= 0 Hz and $(f_s\text{+}f_r)$=2f. -> DC component is measurement goal* (in-phase component, X), the 2f component can be cancelled with an appropriate low-pass filter
- R, Θ_r calculated by transformation from Cartesian to Polar coords

Not discussed here: LP filter characteristics and trade-offs

*contribution from any signal that is not at the same frequency as the reference signal is attenuated close to zero.

📖 EN Wikipedia *Lock-in amplifier; Zurich Instruments Lock-in white paper*

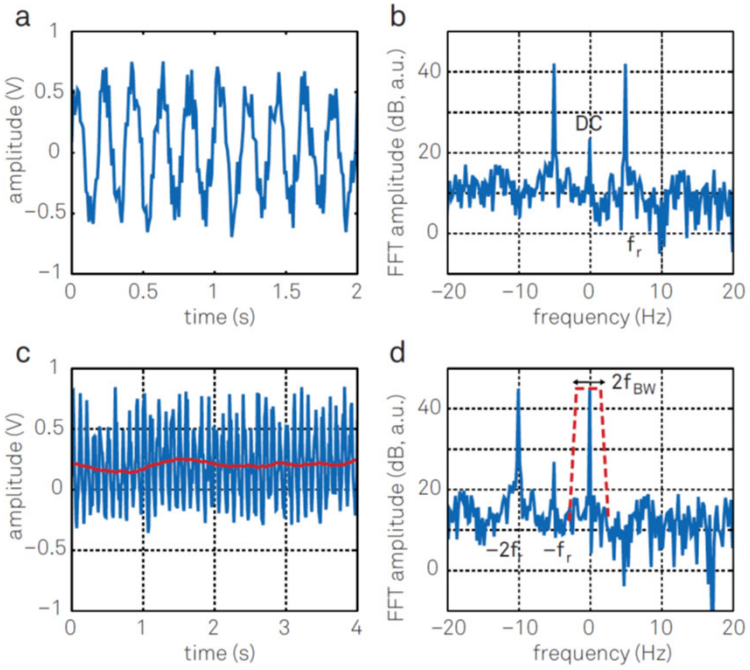
12.1.2 Lock-in Amplifier: Example

(a) TD: Sinusoidal input signal superimposed with noise.

(b) FD: Same represented in the frequency domain (two symmetric peaks + DC component = offset).

(c) TD: After mixing with the reference signal (blue trace) and low-pass filtering (red trace).

(d) FD: the frequency-mixing shifts the frequency components by -f_r. The filter then picks out a narrow band of f_{BW} around zero.



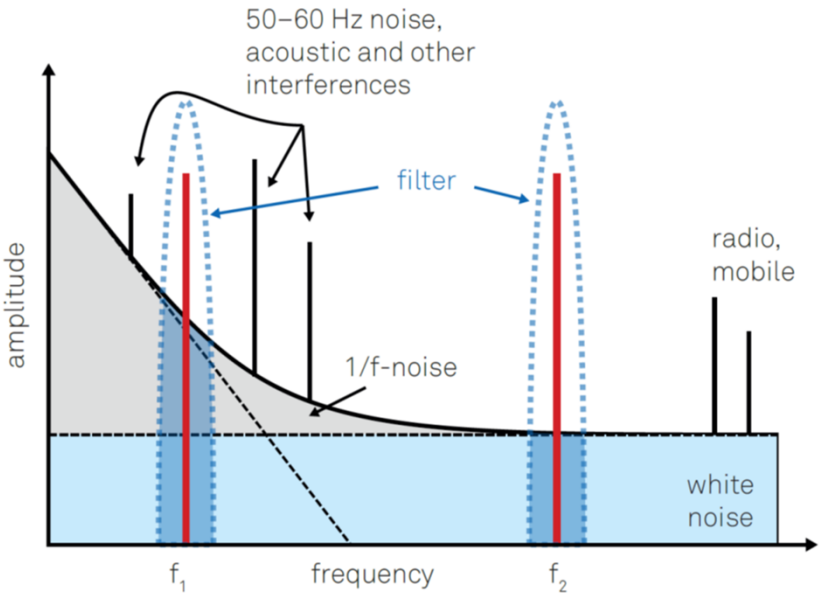
EN Wikipedia *Lock-in amplifier; Zurich Instruments Lock-in white paper*

Q: a component at $-f_r$ appears in the bottom right plot. What do you think that its origin can be?

→ This is probably due to the mixing of the original DC component (which was not included in the previous slide): "-> comes from offset and 1/f noise in the input signal. To obtain accurate measurements this component has to be suppressed by proper filtering."

12.1.2 Lock-in Amplifier: Example

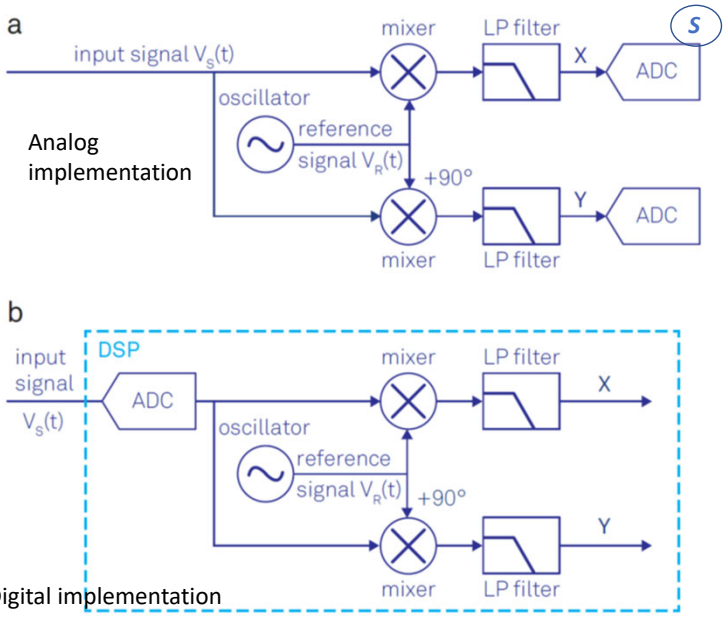
- Qualitative noise spectrum example (typical experiment).
- The measurement frequency should be chosen in a region with small background.
- Here, f_2 will provide better results than f_1 for the same filter bandwidth.



Zurich Instruments Lock-in white paper

12.1.2 Lock-in Amplifier

- Reference signal is usually a sine wave, but not only (e.g. square wave -> captures all odd harmonics).
- NB: when the signal-to-noise ratio is low, a strong, clean reference signal is required, at the same frequency as the received signal. Might not be always available -> instrument limitations.
- Used as precision AC voltage and AC phase meters, noise measurement units, impedance spectroscopes, network analyzers, spectrum analyzers and phase detectors in phase-locked loops.



Digital implementation
(immediate conversion to the digital domain – all subsequent steps are carried out numerically)

EN Wikipedia *Lock-in amplifier; Zurich Instruments Lock-in white paper*

12.1.2 Lock-in Amplifier: Examples

Stanford Research Instruments, Analog Lock-in
By Nuno Nogueira (Nmnogueira) - Self-made, CC BY-SA 2.5, https://en.wikipedia.org/w/index.php?curid=13431432

Zurich Instruments, Digital Lock-in

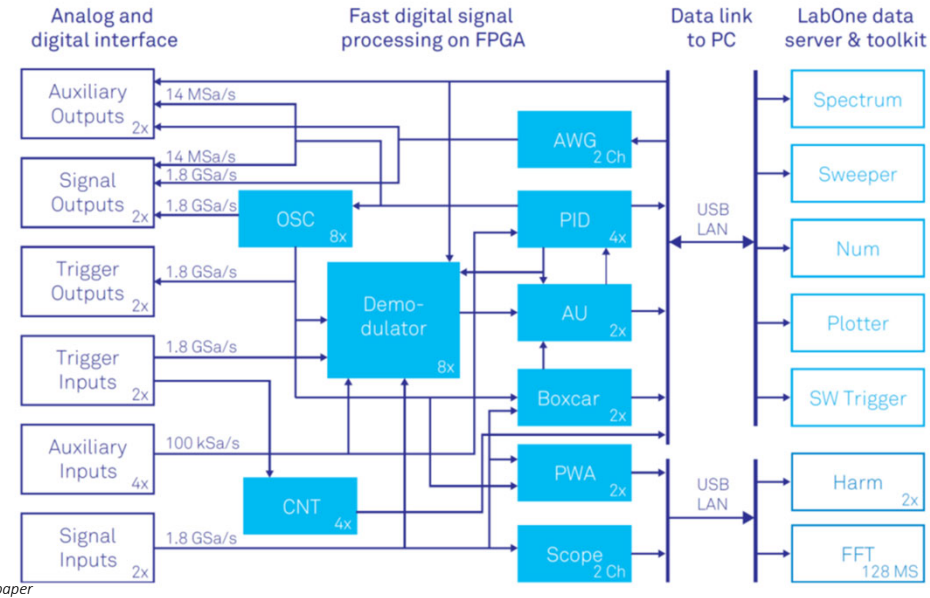
EN Wikipedia *Lock-in amplifier*

12.1.2 Lock-in Amplifier: Example of a digital instrument

Zurich Instruments, block diagramme

Multiple demodulators

-> analyze a signal with different filter settings or at multiple different frequencies simultaneously.



Zurich Instruments Lock-in white paper

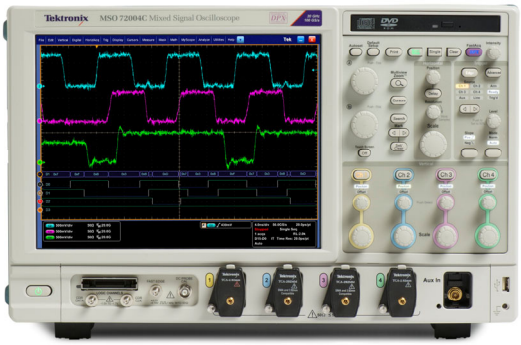
Note the complexity of a modern digital lock-in instrument! Both input as well as output interfaces are possible as well, together with different filtering options and trigger channels. Most of the signal processing is FGPA-based.

kSa/s, Msa/s, Gsa/s: kilo/mega/giga Samples per second.

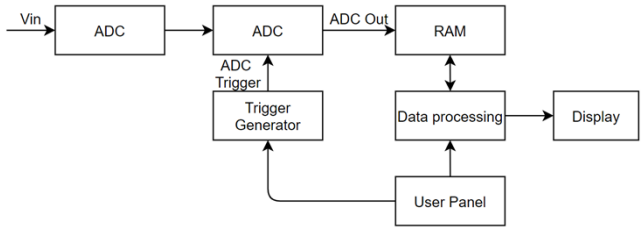
Outline

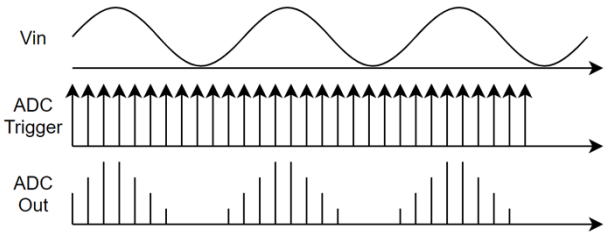
12.1.3 (Digital sampling) Oscilloscope

- They sample and display voltages variations in the time domain.
- Provide different trigger modes to capture the desired signal's variation.
- Provides DFFT operation to analyze the frequency domain.



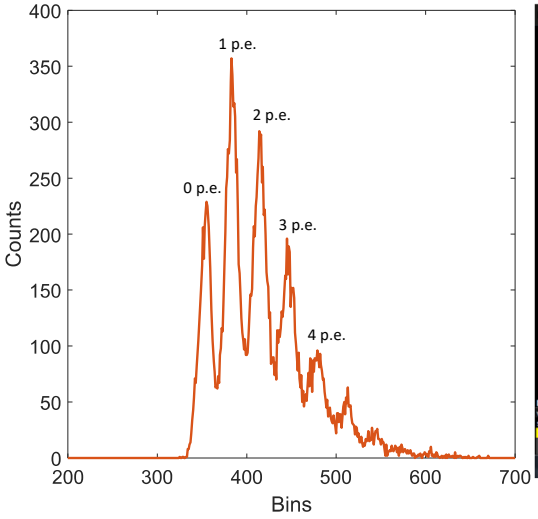
Tektronix, MSO/DPO70000



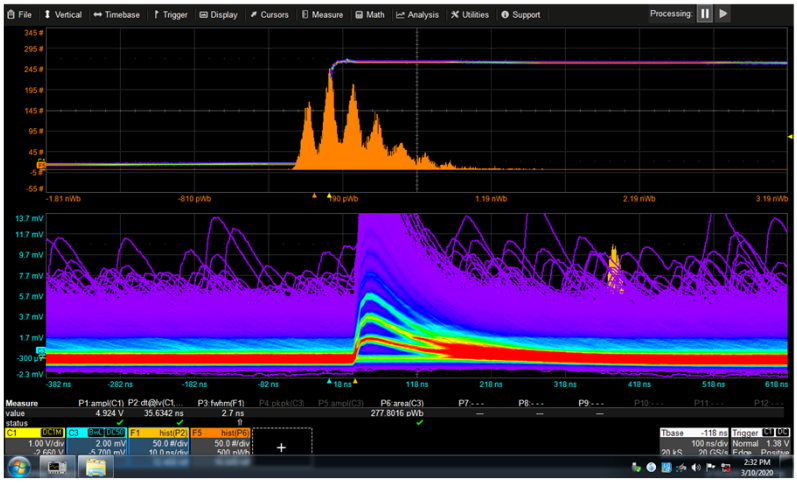


Example: Tektronix MSO72004C - Bandwidth up to 23GHz, 4 Channels, 500Msamples record length, up to 50Gsamples/s

12.1.3 (Digital sampling) Oscilloscope Example



p.e. = photoelectron



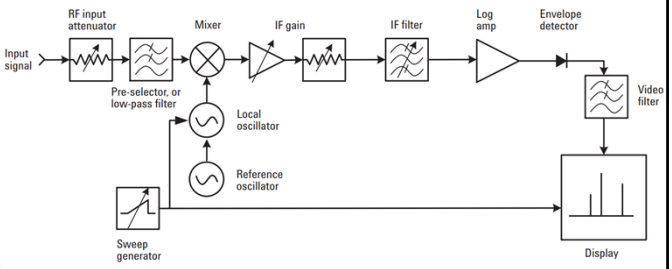
Output signal from an analog silicon photomultipier (SiPM) at very low light levels – "persistence" function allows to visualise very weak but repetitive signals
Courtesy A. Muntean (EPFL-AQUA)

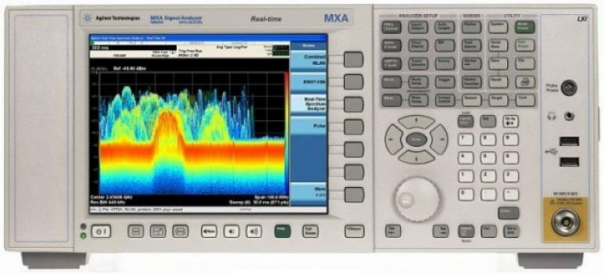
This is an example of an output from an analog silicon photomultiplier (SiPM). Note the possibility of counting individual photons (up to a point) when illuminated with a very weak light source. The corresponding voltage traces are shown in the bottom part of the right plot.

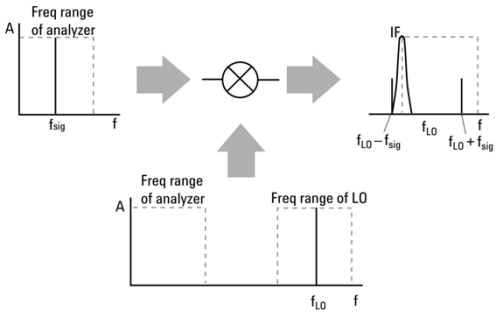
0 p.e. = pedestal (integrated charge due to noise, e.g. leakage current, shot noise, amplifier noise, etc.).

12.1.3 Spectrum Analyzers

- Spectrum analyzers show the frequency domain of a repetitive input signal.
- It uses a frequency sweeper to generate the spectrum frequencies and mixes these frequencies with the input signal.
- Logarithmic amplifier is used to translate the output scale from linear to decibel.







Agilent Spectrum Analysis Basics , Application Note 150, Keysight 26.5 GHz N9020A-RT1

IF = Intermediate Frequency.
IF Gain is coupled with RF input attenuator
IF Filter is selected based on the input frequency range and on the Local Oscillator (LO) maximum frequency.

12.1.3 : Oscilloscopes vs. Spectrum Analyzers

Rule of thumb used to be:

- Frequency-domain measurements (output frequency, band power, signal bandwidth, etc.) -> spectrum analyzer
- Time domain measurements (pulse width and repetition rate, signal timing, etc.) -> oscilloscope
- Nowadays, the lines between these two platforms are blurred –for example, oscilloscopes start incorporating FFT techniques -> frequency-domain data!

https://www.rs-online.com/designspark/do-i-need-a-spectrum-analyzer-or-an-oscilloscope

Outline

Acknowledgments

- Bedirhan Ilik (TA 2019)

Appendix A: PLL – Automobile Race Analogy

- As an analogy of a PLL, consider an auto race with two cars. One represents the input frequency, the other the PLL's output VCO frequency.
- Each lap corresponds to a complete cycle. The number of laps per hour (a speed) corresponds to the frequency. The separation of the cars (a distance) corresponds to the phase difference between the two oscillating signals.
- During most of the race, each car is on its own and free to pass the other and lap the other. This is analogous to the PLL in an unlocked state.

📖 EN Wikipedia *Phase-locked loop;* ***https://en.wikipedia.org/wiki/Phase-locked_loop#Practical_analogies***

Appendix A: PLL – Automobile Race Analogy

- However, if there is an accident, a yellow caution flag is raised. This means neither of the race cars is permitted to overtake and pass the other car.
- The two race cars represent the input and output frequency of the PLL in a locked state.
- Each driver will measure the phase difference (a fraction of the distance around the lap) between himself and the other race car. If the hind driver is too far away, he will increase his speed to close the gap. If he's too close to the other car he will slow down.
- The result is that both race cars will circle the track in lockstep with a fixed phase difference (or constant distance) between them. Since neither car is allowed to lap the other, the cars make the same number of laps in a given time period.
- Therefore the frequency of the two signals is the same.

EN Wikipedia *Phase-locked loop*

Appendix A: PLL – Clock Analogy

- Phase can be proportional to time, so a phase difference can be a time difference. Clocks are, with varying degrees of accuracy, phase-locked (time-locked) to a master clock.
- Left on its own, each clock will mark time at slightly different rates. A wall clock, for example, might be fast by a few seconds per hour compared to the reference clock at NIST. Over time, that time difference would become substantial.
- To keep the wall clock in sync with the reference clock, each week the owner compares the time on his wall clock to a more accurate clock (a phase comparison), and he resets his clock.
- Left alone, the wall clock will continue to diverge from the reference clock at the same few seconds per hour rate.

📖 EN Wikipedia *Phase-locked loop*

Appendix A: PLL – Clock Analogy

- Some clocks have a timing adjustment (a fast-slow control). When the owner compared his wall clock's time to the reference time, he noticed that his clock was too fast.
- Consequently, he could turn the timing adjust a small amount to make the clock run a little slower (frequency).
- If things work out right, his clock will be more accurate than before.
- Over a series of weekly adjustments, the wall clock's notion of a second would agree with the reference time (locked both in frequency and phase within the wall clock's stability).
- An early electromechanical version of a phase-locked loop was used in 1921 in the Shortt-Synchronome clock.

📖 EN Wikipedia *Phase-locked loop*